

PATENT APPLICATION

Sheet 1 of 4

<p>FORM PTO-1449</p> <p>LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT</p> <p align="center">(Use several sheets if necessary)</p>	<p>ATTY. DOCKET NO. 200304950-2</p>	<p>APPLICATION NO.</p>	<p>CONFIRMATION NO.</p>
<p>APPLICANT David Arthur James Webb, Jr. et al.</p>			
<p>FILING DATE</p>		<p>GROUP</p>	

REFERENCE DESIGNATION U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
CH	1A	5,872,946	02/16/99	Narayan et al.	
CH	1B	5,155,843	10/13/92	Stamm et al.	
CH	1C	4,847,755	07/11/89	Morrison et al.	
CH	1D	4,229,790	10/21/80	Gilliland et al.	
CH	1E	6,542,987 B1	04/01/03	Fischer et al.	
CH	1F	5,870,578	02/09/99	Mahalingaiah et al.	
CH	1G	6,115,807	09/05/00	Grochowski	
CH	1H	6,112,019	08/29/00	Chamdani et al.	
CH	1I	5,627,983	05/06/97	Popescu et al.	
CH	1J	5,822,559	10/13/98	Narayan et al.	
CH	1K	6,182,210 B1	01/30/01	Akkary et al.	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	PUBLICATION DATE	NAME OF PATENTEE OR APPLICANT	Pages/Columns/Lines Where Relevant Passages/Figures Appear	Check if Translation attached
/	1L					
/	1M					
/	1N					
/	1O					
/	1P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

CH	1Q	Keller, J., "The 21264: A Superscalar Alpha Processor with Out-of-Order Execution," Paper present at the Microprocessor Forum on October 22-23, 1996
CH	1R	Gieseke, Bruce A. et al., Digital Semiconductor, Digital Equipment Corporation, "A 600MHz Superscalar RISC Microprocessor with Out-Of-Order Execution," ISSCC97/Session 10/High-Performance Microprocessors/Paper FA 10.7, IEEE International Solid-State Circuits Conference, 176-177, 451, (1997).
CH	1S	Farrell, J.A. and Fischer, T.C., "Issue Logic for a 600-MHz Out-of-Order Execution Microprocessor," J. Solid-State Circuits 33(5):707-712 (1998).

<p>EXAMINER</p> <p><i>[Signature]</i></p>	<p>DATE CONSIDERED</p> <p align="center"><i>3/3/05</i></p>
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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	PUBLICATION DATE	NAME	Pages, Columns, Lines Where Relevant Passages or Figures Appear
CH	2A	6,148,394	11/14/00	Tung et al.	
	2B				
	2C				
	2D				
	2E				
	2F				
	2G				
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	2J				
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2L					
2M					
2N					
2O					
2P					

OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, etc.)

CH	2Q	Scott, A.P., et al., "Four-Way Superscalar PA-RISC Processors," J. Hewlett-Packard 1:1-9 (August 1997).
	2R	Farrell, J.A. and Fischer, T.C., "Issue Logic for a 600-MHz Out-of-Order Execution Microprocessor," J. Solid-State Circuits 33(5):707-712 (1998).
	2S	Gwennap, Linley, "Digital 21264 Sets New Standard," Microdesign Resources, Microdesign Report (October 28, 1996).

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3/3/05

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REFERENCE DESIGNATION		U.S. PATENT DOCUMENTS			
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	3A				
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	3L					
	3M					
	3N					
	3O					
	3P					

CH	3Q	A Tour of the P6 Microarchitecture [online], [retrieved on 1999-03-10]. Retrieved from the Internet < URL: http://eecad.sogang.ac.kr/AboutSite+Others/Others/intel/procs/p6/p6white/p6white.htm > .
CH	3R	A 56-Entry Instruction Reorder Buffer [online], [retrieved on 1999-03-10]. Retrieved from the Internet URL: http://www.hp.com/ahp/framed/technology/micropro/micropro/pa-8000/docs/56entry.html > .
CH	3S	Fischer, T. and Leibholz, D., "Design Tradeoffs in Stall-Control Circuits for 600MHz Instruction Queues," Paper presented at the IEEE International Solid-State Circuits Conference (February 1998).

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	4O					
	4P					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

CH	4Q	Kessler, R.E., Compaq Computer Corporation, "The Alpha 21264 Microprocessor," IEEE Micro 24-36 (March-April 1999).
CH	4R	Liebholz, Daniel and Razdan, Rahul, Digital Equipment Corporation, "The Alpha 21264: A 500 MHZ Out-of-Order Execution Microprocessor," from Compcon February, 1997 Proceedings.
CH	4S	Popescu, V. et al., "The Metaflow Architecture," IEEE Micro, Vol. 11, Issue 3, June 1991, pp. 10-13, 63-73.

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